REMARKS/ARGUMENTS

Record of Interview

On May 27, 2004, an interview was conducted by telephone between Examiner Bragdon and Masako Ando, Limited Recognition under 37 CFR §10.9(b). Applicant thanks the Examiner for granting this interview. The details of the interview are set forth in the Interview Summary document made of record, which is attached herewith in the Appendix.

Claim Status and Amendment to the Claims

Claims 1-12 and 14-36 are now pending.

No claims stand allowed.

Claims 1-4, 6, 8-10, 12, 17, 20, 22, 24 and 26 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention. Support for these changes may be found in the specification, page 8, lines 24 and page 9, lines 5-17. The text of claims 5, 7, 11, 14-16, 18-19, 21, 23, 25 and 27-28 is unchanged, but their meaning is changed because they depend from amended claims.

New claims 29-36 also particularly point out and distinctly claim subject matter regarded as the invention. Support for these claims may be found in the specification, page 9, lines 5-17.

The amendment also contains minor changes of a clerical nature.

No "new matter" has been added by the amendment.

Claim Objections

Claims 2, 4-6, 10, 17, 22, and 24-26 stand objected to because of certain informalities as noted in the Office Action. Claims 2, 4, 6, 10, 17, 22, 24 and 26 have been amended in accordance with the Examiner's suggestion.

With this amendment, withdrawal of the objection to the claims is respectfully requested.

The 35 U.S.C. §103 Rejection

Claims 1, 3, 6-9, 11-12, 15-16, 18-21, 23 and 26-28 stand rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Traynor (U.S. Pat. No. 6,263,403) in view of Moore et al. (U.S. Pat. No. 5,437,017), among which claims 1, 8-9, 12 and 20 are independent claims. This rejection is respectfully traversed.

According to M.P.E.P. §2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.

Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Claim 1 defines a method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors. The claimed method comprises (a) accessing a virtual address in a first TLB associated with one of the plurality of processors, (b) performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address, (c) generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address, (d) sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network, and (e) determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message, as recited in claim 1 as amended.

In the Office Action, the Examiner specifically alleges that Traynor's INVALIDATE request teaches the claimed TLB message. However, Applicant respectfully disagrees for the reasons set forth below.

As recited in claim 1 as amended, in the claimed invention, the TLB message is generated in response to a change in contents of the first TLB caused by the operation performed on the first TLB. That is, the contents of the TLB is first changed by the

operation on the TLB itself, and in response to that change, the TLB message is generated and sent to other processors (other TLBs). For example, the contents of the TLB is changed by inputting a new entry to the TLB, modifying or removing an exiting entry in the TLB (referred to as "TLB transaction").

In Traynor, on the other hand, the INVALIDATE request is broadcasted by a module *seeking to modify* the contents of a memory location when employing "snoopy" method (column 4, lines 36-38 thereof), or issued by a cache module that *intends to modify* a memory location when employing directory-based method (column 4, lines 60-62 thereof). The INVALIDATE request is broadcasted to all of the "cache modules" in the snoopy system, or directed to the memory controller which maintains the directory and cache coherency (column 4, lines 37-39, and column 4, line 62 to column 5, line10 thereof). In either case, the INVALIDATE request is issued *before* any access to a TLB, any operation upon the TLB, or any change in the TLB occurs, since the module is seeking to modify the memory contents and actual memory access *using a TLB* has not yet occurred. Thus, the INVALIDATE request of Traynor cannot teach the claimed TLB request which is generated in response to a change in contents of the TLB caused by the operation performed on the first TLB, as recited in claim 1.

In addition, the description of column 6, lines 27-38 in Traynor does not teach or suggest the claimed TLB message, either. In the cited portion, Traynor states as follows:

> In this example, assume that TLB **16** contains a translation for VPN 1, and PAGE_TABLE_BASE is 1A000000H (which is specified in hexadecimal format). Further assume that some other module, such as another CPU or I/O device, seeks to alter the virtual-to-physical translation for VPN 1. The address of the PTE in table **12**

corresponding to VPN 1 is 1A000004. To modify this memory location, the other module will need to gain control of the cache line containing this location.

Here, in the statement: "TLB **16** contains a translation for VPN 1," VPN 1 is a virtual page number (VPN) of the virtual address format shown in FIG. 1. Thus, this statement merely teaches that the TLB **16** contains a translation for the virtual address (into a physical address). The next statement: "PAGE_TABLE_BASE is 1A000000H (which is specified in hexadecimal format)" is regarding to the page table **12** as illustrated in FIG. 2 of Traynor, not the TLB **16** (see column 5, lines 58-62 of Traynor). It should be noted that although a page table (PT) provides the translation between virtual addresses and physical addresses, the PT is not a TLB and is much larger than a TLB. Each page table entry (PTE) typically includes the virtual address and protection/status information concerning the page (column 1, lines 34-38, FIG. 2 of Traynor). Since the page tables are large and thus stored in a main memory, many computer systems use a TLB which is typically a small, fast memory situated on or in close proximity to the processor unit (or other module) and stores recently used pairs of virtual-to-physical address translations in the form of PTEs (column 1, lines 43-52 of Traynor).

The statement: "The address of the PTE in table **12** corresponding to VPN 1 is 1A000004" also refers to an entry in the page table **12**, not an entry or contents of the TLB **16**. In the statement: "To modify this memory location, the other module will need to gain control of the cache line containing this location," the "memory location" is a main memory location identified by the physical address 1A000004, and the "cache line" is a copy of potion of the memory system in a cache memory. Thus, when Traynor

assumes that some other module, such as another CPU or I/O device (i.e., "cache module" as discussed above), seeks to alter the virtual-to-physical translation for VPN 1 (column 6, lines 31-32 thereof), the virtual-to-physical translation is that in the page table **12**, not in the TLB **16**.

Accordingly, the cited portion of Traynor merely describes an example in which a cache module seeks to modify the page table **12**. Then, in Traynor, the cache coherency process continues as follows:

> In a computer system using the snoopy method of cache coherency, the other *cache module* will broadcast a READ_AND_INVALIDATE request, as described above. In a computer system using the directory-based method of cache coherency, the other *cache module* will direct a READ request to the memory controller, and the memory controller will direct an INVALIDATE request *to other modules sharing the cache line.* Note that to implement the present invention in a computer system using the directory-based method, the directory will need to treat any TLB entries as "sharers" of cache lines in the page table, thereby allowing the memory controller to direct INVALIDATE requests to the TLBs. Also note that the computer system may use both protocols in a layered scheme, as described above. (column 6, lines 35-49 of Traynor, *emphasis* added)

Thus, as discussed above, the INVALIDATE request is issued by a cache module seeking to modify the page table, not the TLB, before anything happens in the TLB. Although Traynor treats "any TLB entries as "sharers" of cache lines," this treatment merely allows the INVALIDATE requests to be directed to the TLBs. When the INVALIDATE request issued by the cache module reaches to a TLB (or any module controlling the TLB), an operation, if any, is performed onto the TLB or a change, if any, occurs in the TLB. Such a change is a result of the INVALIDATE request, and the INVALIDATE request is not generated as a result of the change. This is contrary to the

claimed invention where the TLB message is generated in response to a change in contents of the TLB caused by the operation performed on the TLB, as recited in claim 1.

In addition, it should be noted that Traynor's INVALIDATE request is based on cache memory coherency transactions and TLB purges are merely piggy-backed on the existing cache coherency transaction. Since the major advantage of Traynor is using the existing set of cache coherence transactions to maintain TLB coherence without additional transactions, Traynor also fails to suggest desirability to provide an INVALIDATE request (the alleged TLB message) which is generated separately from the cache coherency by independent TLB transactions or in response to any change in contents of the TLB itself as recited in claim 1.

Regarding Moore, the cited portion (column 2, lines 25-30 thereof) merely states, in general, changes in a TLB should be mapped onto other TLBs to maintain TLB coherency, but no suggestion or teaching about how such TLB coherency is implemented. Thus, Moore also fails to teach or suggest the claimed features missing from Traynor.

Accordingly, Traynor, whether considered alone or combined with or modified by Moore, does not teach or suggest generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, as recited in claim 1. Claims 8-9, 12, and 20 includes, among others, substantially the same distinctive features as claim 1.

It is respectfully requested that the rejection of claims based on Traynor and Moore be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-7, 19 and 28 depend from claim 1, claims 10-11 depend from claim 9, claims 14-18 depend from claim 12, and claims 21-27 depend from claim 20, and thus include the limitations of the corresponding independent claims. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reasons.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-1698.

Respectfully submitted,
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Masako Ando
Limited Recognition under 37 CFR §10.9(b)

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